Generating power-optimal standard cell library specification using neural network technique

ABSTRACT

In VLSI semi-custom design approach, power-optimal standard cell library selection for a given block design requires time-consuming iterative processes. This paper presents a framework to select a standard cell library that can result in near-optimal power while satisfying targeted frequency. The framework relies on neural network model to quickly predict the total power of a block design associated with a given standard cell library in order to speed up the synthesis process. The experimental result based on various synthesized benchmark circuits demonstrated the effectiveness of proposed framework for near-optimal standard cell library specification.

Keyword: Neural network; Power optimization; Standard cell library